Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-6 (Canceled)

7 (Previously Presented) A method for processing signals on a programmable logic device that includes a plurality of programmable logic regions, the method comprising:

configuring at least one of the regions as word conditioning logic;

configuring at least another one of the regions as a computation unit having an input, an output, and a critical path, wherein the computation unit is configured to propagate signals from the input to the output via the critical path without propagating the signals through the word conditioning logic;

providing a datapath from the output of the computation unit to a storage destination, wherein signals

on the datapath are propagated through the word conditioning logic; and

configuring at least a further one of the regions as analysis logic.

8 (Original) The method defined in claim 7, further comprising:

performing an analysis operation in the analysis logic in combination with a write operation to the storage destination.

9 (Original) The method defined in claim 7, further comprising:

performing an analysis operation in the analysis logic in combination with a move operation to the storage destination.

10 (Original) The method defined in claim 7, wherein the analysis logic is configured to perform block floating point analysis.

11-17 (Canceled)

18 (Previously Presented) A programmable logic device, comprising:

a computation unit having an input, an output, and a critical path, wherein the computation unit is configured to propagate signals received on the input to the output via the critical path without propagating the signals through word conditioning logic;

a datapath configured to convey output signals from the computation unit to a storage destination, wherein the output signals on the datapath are propagated through word conditioning logic; and

a second logic substructure containing analysis logic and having an associated input and an associated output, wherein the associated input of the second logic substructure is coupled to the datapath.

19 (Original) The device defined in claim 18, wherein the analysis logic contained in the second logic

substructure is configured to perform block floating point analysis.

20 (Original) The device defined in claim 18, wherein the analysis logic contained in the second logic substructure is executable in combination with a write operation to the storage destination.

21 (Original) The device defined in claim 18, wherein the analysis logic contained in the second logic substructure is executable in combination with a move operation to the storage destination.

22 (Currently Amended) A digital processing system, comprising:

processing circuitry;

a system memory coupled to said processing circuitry; and

the device defined in claim ~~11~~ 18 coupled to the processing circuitry and the system memory.

23 (Currently Amended) A printed circuit board on which is mounted the device defined in claim ~~11~~ 18.

24 (Original) The printed circuit board defined in claim 23, further comprising:

a board memory mounted on the printed circuit board and coupled to the device.

25 (Original) The printed circuit board defined in claim 23, further comprising:

processing circuitry mounted on the printed circuit board and coupled to the device.

26-27 (Canceled)

28 (Previously Presented) A programmable logic integrated circuit device including a plurality of programmable logic regions, the device comprising:

a storage circuit;

at least one region configured as a data conditioning and analysis circuit, wherein the data conditioning and analysis circuit comprises at least one

word conditioning subcircuit and at least one analysis subcircuit, wherein the data conditioning and analysis circuit is configured to be programmably selectively operable in a plurality of alternative modes, wherein in a first mode, the word conditioning subcircuit is in operation, and wherein in a second mode, the analysis subcircuit is in operation;

at least another region configured as a computation circuit having an input, an output, and a critical path, wherein the computation circuit is configured to propagate signals received on the input to the output via the critical path without propagating the signals through the data conditioning and analysis circuit, and wherein the computation circuit is programmably selectively configurable to perform at least one arithmetic operation on input data supplied from the storage circuit to produce output data; and

a datapath configured to convey the output data from the computation circuit to the storage circuit, wherein the output data on the datapath are propagated through the data conditioning and analysis circuit.

29 (Previously Presented) A programmable logic integrated circuit device including a plurality of programmable logic regions, the device comprising:

a storage circuit;

at least one region configured as a data conditioning and analysis circuit, wherein the data conditioning and analysis circuit comprises at least one word conditioning subcircuit and at least one analysis subcircuit, wherein the word conditioning subcircuit is configured to be operated in series with the analysis subcircuit;

at least another region configured as a computation circuit having an input, an output, and a critical path, wherein the computation circuit is configured to propagate signals received on the input to the output via the critical path without propagating the signals through the data conditioning and analysis circuit, and wherein the computation circuit is programmably selectively configurable to perform at least one arithmetic operation on input data supplied from the storage circuit to produce output data; and

a datapath configured to convey the output data from the computation circuit to the storage circuit, wherein the output data on the datapath are propagated through the data conditioning and analysis circuit.

30 (Previously Presented) A programmable logic integrated circuit device including a plurality of programmable logic regions, the device comprising:

a storage circuit;

at least one region configured as a data conditioning and analysis circuit, wherein the data conditioning and analysis circuit comprises:

rounding logic;

saturation logic; and

block floating point analysis logic;

at least another region configured as a computation circuit having an input, an output, and a critical path, wherein the computation circuit is configured to propagate signals received on the input to the output via the critical path without propagating the signals through the data conditioning and analysis circuit, and wherein the computation circuit is programmably selectively configurable

to perform at least one arithmetic operation on input data supplied from the storage circuit to produce output data; and

a datapath configured to convey the output data from the computation circuit to the storage circuit, wherein the output data on the datapath are propagated through the data conditioning and analysis circuit.

31-34 (Canceled)

35 (New) The method defined in claim 7, further comprising:

providing rounding logic in the word conditioning logic.

36 (New) The method defined in claim 7, further comprising:

providing saturation logic in the word conditioning logic.

37 (New) The method defined in claim 7, further comprising:

providing rounding logic and saturation logic in the word conditioning logic, wherein the rounding logic and the saturation logic are arranged in series.

38 (New) The method defined in claim 37, further comprising:

monitoring the signals in the computation unit using the saturation logic.

39 (New) The method defined in claim 38, wherein the monitoring is performed by monitoring circuitry included in the saturation logic, wherein the monitoring circuitry is operated separately from and in parallel with the computation unit.

40 (New) The device defined in claim 18, wherein the computation unit includes an arithmetic logic unit in the critical path, wherein the arithmetic logic unit does not include word conditioning logic.

41 (New) The device defined in claim 18, wherein the computation unit includes an accumulator in the critical

path, wherein the accumulator does not include word conditioning logic.

42 (New) The device defined in claim 18, further comprising:

a first logic substructure containing word conditioning logic and having an associated input and an associated output, wherein the associated input of the first logic substructure is coupled to the output of the computation unit and the associated output of the first logic substructure is coupled to the datapath.

43 (New) The device defined in claim 42, wherein the word conditioning logic contained in the first logic substructure is configured to perform rounding and saturation operations.

44 (New) The device defined in claim 18, further comprising:

a plurality of memory circuits, wherein the storage destination is at least one of the plurality of memory circuits.

45 (New) The device defined in claim 18, further comprising:

a plurality of registers, wherein the storage destination is at least one of the plurality of registers.

46 (New) The device defined in claim 28, wherein the data conditioning and analysis circuit comprises at least one word conditioning subcircuit and at least one analysis subcircuit.

47 (New) A digital processing system, comprising:

processing circuitry;

a system memory coupled to said processing circuitry; and

the device defined in claim 28 coupled to the processing circuitry and the system memory.

48 (New) A printed circuit board on which is mounted the device defined in claim 28.

49 (New) The printed circuit board defined in claim 48, further comprising:

a board memory mounted on the printed circuit board and coupled to the device.

50 (New) The printed circuit board defined in claim 48, further comprising:

processing circuitry mounted on the printed circuit board and coupled to the device.

51 (New) The device defined in claim 28, wherein the data conditioning and analysis circuit comprises at least one word conditioning subcircuit and at least one analysis subcircuit.

52 (New) The device defined in claim 29, wherein the data conditioning and analysis circuit comprises at least one word conditioning subcircuit and at least one analysis subcircuit.

53 (New) The device defined in claim 30, wherein the data conditioning and analysis circuit comprises at least

one word conditioning subcircuit and at least one analysis subcircuit.